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comprising the steps of:

forming a crystalline semiconductor film over a substrate;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film comprising silicon oxide on each of said first and second semiconductor islands by a vapor phase deposition using TEOS;

irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas; and

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

REMARKS

The Office Action of **September 17, 2001**, has been received and its contents carefully noted. Applicant respectfully submits that this response is timely filed and fully responsive to the Office Action. Claims 1-14 and 29-37 were pending in the present application prior to the aforementioned amendment. By the above amendment, claims 1, 6, 11, 30, and 34 are amended to more clearly define subject matter which Applicant was already entitled. Because the amended claim language is supported at least on pages 13-17 of the specification and Figures 1A-1E of the drawings, Applicant submits that no issue of new matter is raised by this amendment. Accordingly, claims 1-14 and 29-37 are still pending in the present application and, at least for the reasons set forth below, are believed to be in condition for allowance.

Initially, the Examiner finds that the information submitted in the Information Disclosure Statements filed November 10, 1999 and February 16, 2000 allegedly fail to

comply with 37 C.F.R. §1.98(a)(2), and thus, are not being considered. Applicant traverses this finding in that the information submitted in the IDS of February 16, 2000 was previously acknowledged as considered by the Examiner on March 14, 2001. Appendix A contains a copy of the initialed copy of the Form PTO 1449 of February 16, 2000. Accordingly, the issue regarding the alleged non-compliance with the Rules concerning the IDS of February 16, 2000 should be moot.

With regard to the Information Disclosure Statement filed November 10, 1999, Applicant respectfully contends that this IDS is appropriate under the Rules and, thus, should be considered inasmuch as it falls within the exception to the IDS requirement for copies of the submitted information. M.P.E.P. §609 (August 2001). Specifically, 37 C.F.R. §1.98(d) provides that:

A copy of any patent, publication, pending U.S. application, or other information listed in an information disclosure statement is not required to be provided if: (1) the information was previously cited by or submitted to, the Office in a prior application, provided that the prior application is properly identified in the IDS and is relied on for an earlier filing date under 35 U.S.C. 120; and (2) the IDS submitted in the earlier application complies with 37 C.F.R. 1.98(a)-(c). If both of these conditions are met, the examiner will consider the information previously cited or submitted to the Office and considered by the Office in a prior application relied on under 35 U.S.C. 120.

Applicant submits that the subject application complies with the first nexus of 37 C.F.R. §1.98(d) since the November 10, 1999 IDS included a statement that the information listed in the Form PTO 1449 was cited in applications relied upon for domestic priority under 35 U.S.C. 120, namely, parent Application Serial No. 08/721,526 (now U.S. Patent No. 6,169,980), and its predecessor, Application Serial No. 08/111,522 (now abandoned). Further, as can be readily seen in Appendix B, each of the cited references in the IDS of November 10, 1999 were either submitted by Applicant or cited by the Office during prosecution of the '980 patent and '522 application.

Applicant further submits that the subject application complies with the second nexus of 37 C.F.R. §1.98(d) since the information contained in the IDS of November 10, 1999 was previously considered by the Office. Appendix B contains initialed copies of Forms PTO 1449 and copies of PTO 892s that were considered by the Office during prosecution of the '980 patent and the '522 application. Accordingly, the fact that each item of information cited in the Form PTO 1449 were initialed by the Office indicates that the IDS's were in conformance with the requirements of 37 C.F.R. §1.98. Consequently, the Examiner is obligated under 37 C.F.R. §1.98(d) to consider the information contained in the IDS of November 10, 1999.

It is not understood why the Examiner would indicate that Applicant's failed to comply with the Rules, when in fact, as the aforementioned argument sets forth, the black letter of the Rules were followed. Applicant understands that the integrity of the PTO filewrappers are sometimes compromised, and for the sake of prosecutorial expediency, Applicant is more than willing to assist the Patent Office in such an occurrence and will submit these copies for the Examiner's convenience, shortly. Applicant should not, however, be cited by the Examiner as being non-compliant with the Rules.

The Office Action maintains the rejections of claims 1-4, 6-9 and 30-33 under 35 U.S.C. §103(a) as unpatentable over *Applicant's Admitted Prior Art* (hereinafter "*APA*") in view of either *Ang et al.* ("Electrical characterization of low-pressure chemical-vapor-deposited silicon dioxide metal-oxide-silicon structures" Journal of Applied Physics 73(5) pp. 2397-2401, 1 March 1993), claims 1-4, 6-9, 11-13, 29, 30-33 and 34-37 under 35 U.S.C. §103(a) as unpatentable over *APA* in view of *Roy* (U.S. Patent No. 5,153,701) and *Wolf* (Silicon Processing for the VLSI Era, Vol. 1, Lattice Press: Sunset Beach, CA, 1986, pp. 57-58) or *JP 58-098933*, and claims 5, 10 and 14 under 35 U.S.C. §103(a) as unpatentable over *APA* in view of *Ang et al.* or *Roy* and *Wolf*, or *Roy* and *JP 58-098933*, and further in view of *JP 60-187030*.

The claimed invention is directed to a method of manufacturing a semiconductor device, including, *inter alia*, steps of forming a semiconductor film comprising amorphous silicon over a substrate, crystallizing the semiconductor film by irradiating a laser light, patterning the crystallized semiconductor film to form first and second semiconductor islands, forming an insulating film on each of the first and second semiconductor islands by a vapor phase deposition, irradiating an intense light to the insulating film in an atmosphere comprising an oxygen gas, forming a gate electrode on the insulating film, introducing phosphorus into the first and second semiconductor islands, and introducing boron into the second semiconductor island such that a dose amount of the boron is larger than that of the phosphorus.

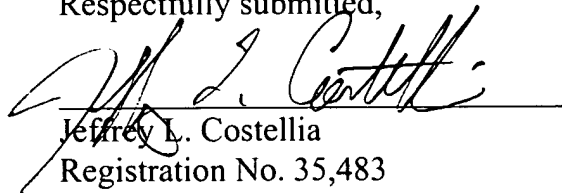
As the Examiner well knows, three criteria must be met in order to establish a *prima facie* case of obviousness. *M.P.E.P.* §2143 (August 2001). Initially, there must be some teaching, suggestion, or motivation to combine or modify the teachings of the prior art to produce the claimed invention, found either in the references themselves or in the knowledge generally available to a skilled artisan. *In re Fine*, 837 F.2d 1071, 5 USPQ.2d 1596 (Fed. Cir. 1988). Secondly, there must be a reasonable expectation of success. *In re Rhinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976). And lastly, the prior art must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

Applicant respectfully contends that the claims as presently pending define subject matter which is clearly patentably distinct over the prior art of record. More particularly, Applicant respectfully contends that the *APA*, either alone or in combination with at least one of *Ang et al.*, *JP 60-187030*, *Roy*, *Wolf*, *JP-58-098933* and *JP 60-187030*, fails to expressly teach or inherently suggest all of the limitations presently set forth in the claimed invention necessary to support a *prima facie* case of obviousness under §103.

Referring now to the rejection, while the Office Action finds that the proposed *APA* modifications teaches a method of manufacturing a semiconductor device using various method steps, it is contended that the respective disclosures set forth in the proposed *APA* modifications fail to expressly teach or inherently disclose a method of manufacturing a semiconductor device by performing steps that result in the formation of an N-channel thin film transistor and a P-channel thin film transistor, as presently set forth at least in independent claims 1, 6, 11, 30 and 34. In particular, the combined teachings of the proposed *APA* modifications fail to provide a method of manufacturing a semiconductor device by introducing phosphorus into first and second semiconductor islands, and introducing boron into the second semiconductor island such that a dose amount of the boron is larger than that of the phosphorus.

Accordingly, since neither of the proposed *APA* modifications expressly teaches or implicitly suggests the disclosed features of the present invention, and also fail to recognize the unobvious advantages first proposed by Applicant, Applicant respectfully requests favorable reconsideration and withdrawal of the §103 rejections. Should the Examiner deem that a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,



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Marked-up copy of amended claims.

1. (Thrice Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising amorphous silicon over a substrate;

crystallizing said semiconductor film by irradiating a laser light;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film on [the crystallized semiconductor film] each of said first and second semiconductor islands by a vapor phase deposition; [and]

irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas [under a pressure of 10 Torr or less.];

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

6. (Thrice Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising amorphous silicon over a substrate;

crystallizing said semiconductor film by irradiating a laser light;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film comprising silicon oxide on [the crystallized semiconductor film] each of said first and second semiconductor islands by a vapor phase deposition; [and]

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irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas [under a pressure of 10 Torr or less.];

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

11. (Thrice Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising amorphous silicon over a substrate;

crystallizing said semiconductor film by irradiating a laser light;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film comprising silicon oxide on [the crystallized semiconductor film] each of said first and second semiconductor islands by a vapor phase deposition using TEOS; [and]

irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas [under a pressure of 10 Torr or less.];

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

30. (Thrice Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a crystalline semiconductor film over a substrate;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film comprising silicon oxide on [said crystalline semiconductor film] each of said first and second semiconductor islands by a vapor phase deposition; [and]

irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas [under a pressure of 10 Torr or less.];

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

34. (Thrice Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a crystalline semiconductor film over a substrate;

patterning the crystallized semiconductor film to form first and second semiconductor islands;

forming an insulating film comprising silicon oxide on [said crystalline semiconductor film] each of said first and second semiconductor islands by a vapor phase deposition using TEOS; [and]

irradiating an intense light to said insulating film in an atmosphere comprising an oxygen gas [under a pressure of 10 Torr or less.]; and

forming a gate electrode on said insulating film;

introducing phosphorus into said first and second semiconductor islands; and

introducing boron into said second semiconductor island,

wherein a dose amount of said boron is larger than that of said phosphorus.

Sheet 1 of 1

Serial N . 09/437,135

Group:

(Use several sheets if necessary)

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	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
EK	63-211759	09/02/88	Japan				
EK	49-78483	07/29/74	Japan				

3/14/07

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Sheet 1 of 1

Form PTO-1449
(Rev. 8-83)U.S. Department of Commerce
Patent and Trademark Office

Attorney Docket No. 0756-1576

Serial No. 08/721,526

Applicant: Shunpei YAMAZAKI et al.

Filing Date: Sept 26, 1996

Group: 2813

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)
EX	5,313,075	05/17/94	Zhang et al	—	—	
EX	5,523,240	06/04/96	Zhang et al	—	—	

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	Document Number	Date	Country	Class	Subclass	Translation Yes N
EX	1-238024	09/22/89	Japan	—	—	Abstract
	2-224253	09/06/90	Japan	—	—	Abstract
	3-34434	02/14/91	Japan	—	—	Abstract
	3-132041	06/05/91	Japan	—	—	Abstract
	4-110470	04/10/92	Japan	—	—	Abstract
	4-165679	06/11/92	Japan	—	—	Abstract
	58-98933	06/13/83	Japan	—	—	Abstract
	60-241269	11/30/85	Japan	—	—	Abstract
	62-119974	06/01/87	Japan	—	—	Abstract
EX	63-105970	05/11/88	Japan	—	—	Abstract
EX	EP 0 459 763	05/02/97	Europe	—	—	

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Examiner

Eis/Katzi

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Submitted with IDS of August 8, 2000

Notice of References CitedApplication No.
08/721,526Applicant(s)
YamazakiExaminer
Matthew WhippleGroup Art Unit
2813

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A	5,970,384	10/99	Yamazaki	438	795
B					
C					
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X	A	5,773,325	6/98	Teramoto	438	151
X	B	5,237,188	8/93	Iwai	257	325
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PTO-1449
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08/721,526

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<i>mi</i>	5,712,191	01/27/98	Nakajima et al.			
<i>mi</i>	5,756,364	05/26/98	Tanaka et al.			
<i>mi</i>	5,773,327	06/30/98	Yamazaki et al.			

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(83)U.S. Department of Commerce
Patent and Trademark OfficeAtty. Docket No.
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ML	5,643,826	07/01/97	Ohtani et al.			
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9/17/98

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8-83)U.S. Department of Commerce
Patent and Trademark OfficeAtty. Docket No.
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mm	5,604,360	02/18/97	Zhang et al.			
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G. Liu et al., "Polycrystalline silicon thin film transistors on Corning 7059 glass substrates using short time, low-temperature processing", American Institute of Physics, 2554-2556.

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ML	4,727,044	02/23/88	Yamazaki			
ML	5,010,037	04/23/91	Lin et al.			
ML	5,075,259	12/24/91	Moran			
ML	5,298,075	03/29/94	Lagendijk et al.			
ML	5,403,772	04/04/95	Zhang et al.			
ML	5,422,311	06/06/95	Woo			
ML	5,426,064	06/20/95	Zhang et al.			
ML	5,481,121	01/02/96	Zhang et al.			
ML	5,488,000	01/30/96	Zhang et al.			
ML	5,492,843	02/20/96	Adachi et al.			

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55-153339	11/29/80	Japan			X Ab
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Examiner	Date Considered 9/17/98

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(Rev. 8-83)

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U.S. Department of Commerce
Patent and Trademark Office

Attorney Docket No. 0756-1576

Serial No. 08721,526

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Applicant: Shunpei YAMAZAKI et al.

Filing Date: Sept. 26, 1996

Group: 2813

U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
WJ	61-89621	05/07/86	Japan			Abstract	
WJ	61-166074	07/26/86	Japan			Abstract	
WJ	EP 0 178 447	04/23/86	Europe			Full & Abstract	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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08/721,526Applicant
Shunpei YAMAZAKI et al.Filing Date
September 26, 1996Group
1104

INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)
<i>mm</i>	4,851,370	07/25/89	Doklan et al.	437	225	
<i>mm</i>	5,476,802	12/19/95	Yamazaki et al.	437	21	

FOREIGN PATENT DOCUMENTS

Document Number	Date	Country	Class	Subclass	Translation Yes No
<i>mm</i> 5-55246	08/26/91	JAPAN			ABS

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

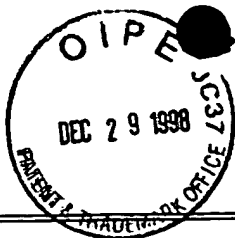
<i>mm</i>	C. Hayzelden et al. "In situ transmission electron microscopy studies of silicide-mediated crystallization of amorphous silicon", (3 pages).

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Sheet 1 of 1

Form PTO-1449
(Rev. 8-83)U.S. Department of Commerce
Patent and Trademark OfficeAtty.Docket No.
0756-1576Serial No.
08/721,526

INFORMATION DISCLOSURE STATEMENT

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Applicant
Shunpei YAMAZAKI et al.Filing Date
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<i>m</i>	4,851,370	07/25/89	Doklan et al.	437	225	
<i>m</i>	5,476,802	12/19/95	Yamazaki et al.	437	21	

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Attorney Docket No. 0756-1576

S rial No. 08/721,526

INFORMATION DISCLOSURE STATEMENT

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Notice of References Cited

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Applicant(s)
Yamazaki et al.

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1104

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